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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/578,007	05/02/2006	Bo-Sung Kim	SAM-OPP052589US	6587

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EXAMINER	
HARRISON, MONICA D	
ART UNIT	PAPER NUMBER
2893	

MAIL DATE	DELIVERY MODE
09/30/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/578,007	KIM ET AL.	
	Examiner	Art Unit	
	Monica D. Harrison	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/2/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Examiner acknowledges claim 3 is cancelled.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in the Republic of Korea on 2/9/04. It is noted, however, that applicant has not filed a certified copy of the 10-2004-0008346 application as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 4-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al (6,100,954).

3. Regarding claim 1, Kim et al discloses a thin film transistor array panel comprising: a substrate (Figure 15B, reference 111); a gate electrode formed on the substrate (Figure 15B, reference 113); a gate insulating layer covering the gate electrode and the substrate (Figure 15B, reference 157); a source electrode and a drain electrode formed on the gate insulating layer (Figure 15B, references 123 and 127); an organic semiconductor layer formed on the gate insulating layer and the source electrode and the drain electrode (Figure 15B, reference 119); and a passivation layer covering the semiconductor layer, the source electrode, the drain electrode, and the gate insulating layer (Figure 15B, reference 159), wherein at least one of the gate insulating layer and the passivation layer is made of Parylene (column 15, lines 14-23).

4. Regarding claim 2, Kim et al discloses wherein the substrate is made of one material selected from plastic, glass, and metal (column 16, lines 45-50)

5. Regarding claim 4, Kim et al discloses a pixel electrode formed on the passivation layer and connected to the drain electrode through a contact hole of the passivation layer that exposes a portion of the drain electrode (Figure 15C, reference 131).

6. Regarding claim 5, Kim et al discloses a manufacturing method of a thin film transistor array panel comprising: forming a gate electrode (Figure 15B, reference 113) on a substrate (Figure 15B, reference 111); forming a gate insulating layer covering the gate electrode on the substrate (Figure 15B, reference 157); forming a source electrode and a drain electrode on the gate insulating layer (Figure 15B, references 123 and 127); forming an organic semiconductor layer covering the source electrode and a portion of the drain electrode (Figure 15B, reference 119); and forming a passivation layer covering the gate insulating layer, the source electrode, the drain electrode, and the organic semiconductor layer (Figure 15B, reference 159), wherein at least one of the gate insulating layer and the passivation layer is made of Parylene (column 15, lines 14-23).

7. Regarding claim 6, Kim et al discloses wherein the gate insulating layer or the passivation layer is made of Parylene by chemical vapor deposition (column 19, lines 43-65).

8. Regarding claim 7, Kim et al discloses a thin film transistor comprising: a substrate (Figure 15B, reference 111); a gate electrode formed on the substrate (Figure 15B, reference 113); a gate insulating layer covering the substrate and the gate electrode (Figure 15B, reference 157); an organic semiconductor layer formed on the gate insulating layer and disposed on the corresponding portion of the gate electrode (Figure 15B, reference 119); a source

electrode and a drain electrode contacting portions of the organic semiconductor layer, formed on the gate insulating layer, and separated by a predetermined distance (Figure 15B, references 123 and 127); and a passivation layer covering the organic semiconductor layer, the gate insulating layer, the source electrode, and the drain electrode (Figure 15B, reference 159), wherein at least one of the gate insulating layer and the passivation layer is made of Parylene (column 15, lines 14-23).

9. Regarding claim 8, Kim et al discloses a thin film transistor array panel comprising: a substrate (Figure 15C, reference 111); a source electrode and a drain electrode formed on the substrate and separated by a predetermined distance (Figure 15C, references 123 and 127) ; an organic semiconductor layer covering the source electrode and the drain electrode (Figure 15C, reference 119); a gate insulating layer covering the substrate and the organic semiconductor layer (Figure 15C, reference 157); a gate electrode formed on the gate insulating layer and disposed on the corresponding portion between the source electrode and the drain electrode (Figure 15C, reference 119); and a passivation layer covering the gate insulating layer and the gate electrode (Figure 15C, reference 159), wherein at least one of the gate insulating layer and the passivation layer is made of Parylene (column 15, lines 14-23).

9. Regarding claim 9, Kim et al discloses a pixel electrode formed on the passivation layer and connected to the drain electrode through a contact hole of the gate insulating layer and the passivation layer that exposes a portion of the drain electrode (Figure 15C, reference 131).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is (571)272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Monica D. Harrison/
Examiner, Art Unit 2893

mdh
September 23, 2008

/Davienne Monbleau/
Supervisory Patent Examiner, Art Unit 2893